**Run 1: Understanding the trainer board**

The power supply is a source of regulated DC power. It is used to power different ICs. It is also used to provide logic level inputs to different digital circuits. Below are the tasks to perform:

**Q:** Why is it called multi-output supply?

**A: Because we have more than one voltage output in trainer board.**

**Q:** Which amongst the outputs of the power supply would you choose for digital IC based experiments? Why?

**A: 5V, otherwise it’ll get damaged. Works best on 5V**

**Run 2: Understanding the CRO**

The CRO is the most useful and versatile electronic test equipment. It lets us see voltage in a circuit as a function of time, triggering on a particular point of the waveform so that a stationary display result. Below are the tasks to perform:

**Q:** Draw the test square waveform generate by CRO itself. What is the voltage and frequency of this waveform?

**A:**

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**Q:** Generate a square wave of 5 V, 1KHz from trainer board to CRO. Calculate its time period and Draw the waveform? Draw another wave form with 2KHz frequency.

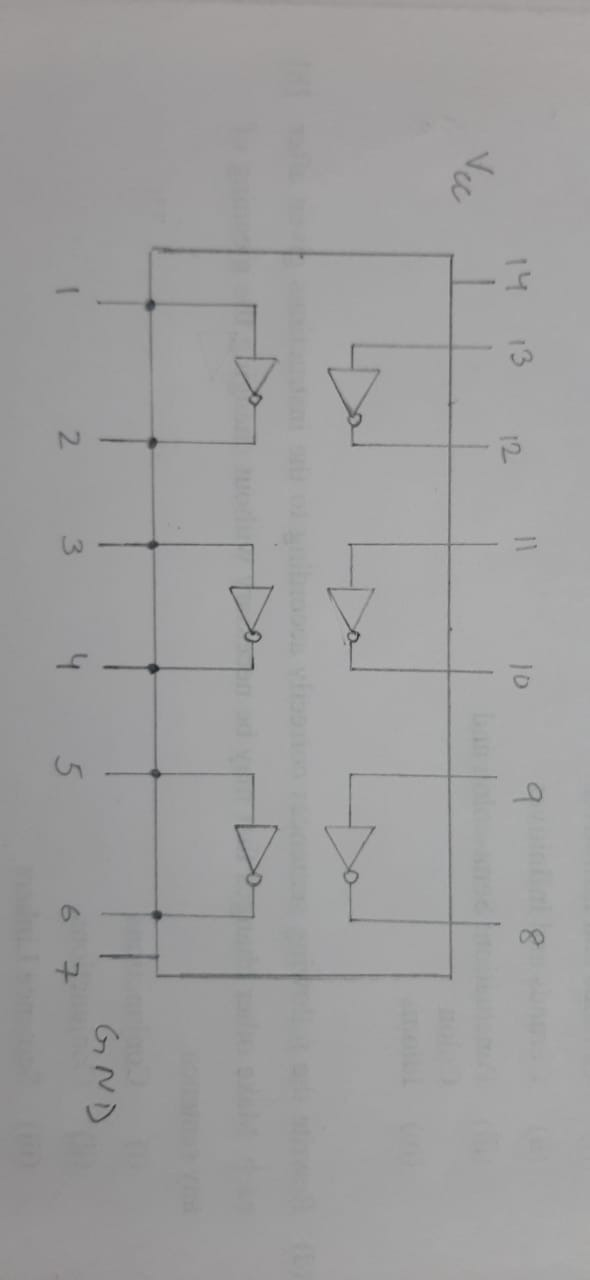
**A:**

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**Run 3: Understanding the IC data sheet of NOT Gate**

**Q:** Write is the IC no. of NOT Gate? Draw its Pin Diagram?

**A: IC number of not gate: 7404**



**Q:** How much voltage is required to operate an IC and write the voltage tolerance?

**A: 5V is required to operate an IC**

**Tolerance 4.75 – 5.25 V**

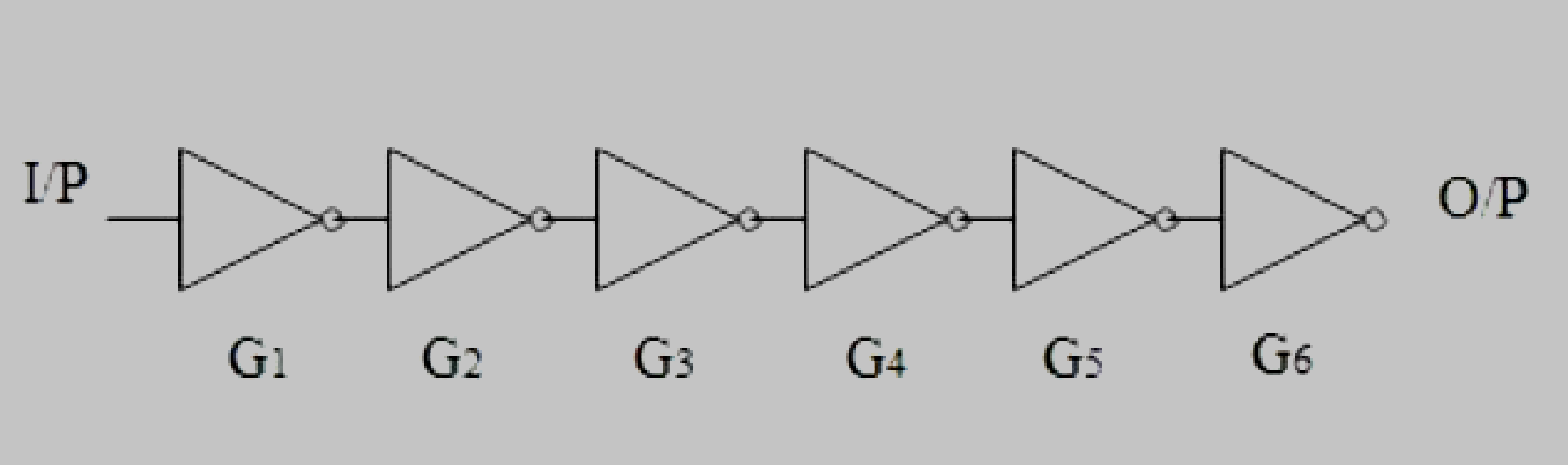
**Q:** Why we connect VCC and Ground?

**A: We connect VCC and Ground for power supply return. Ground acts as a reference.**

**Q:** This IC is belonging to which family and What is the Logical low and high range of it?

**A: IC belongs to 7400 series IC. Low: 0, High: 5.**

**Run 4: Propagation delay of gates using NOT Gate**



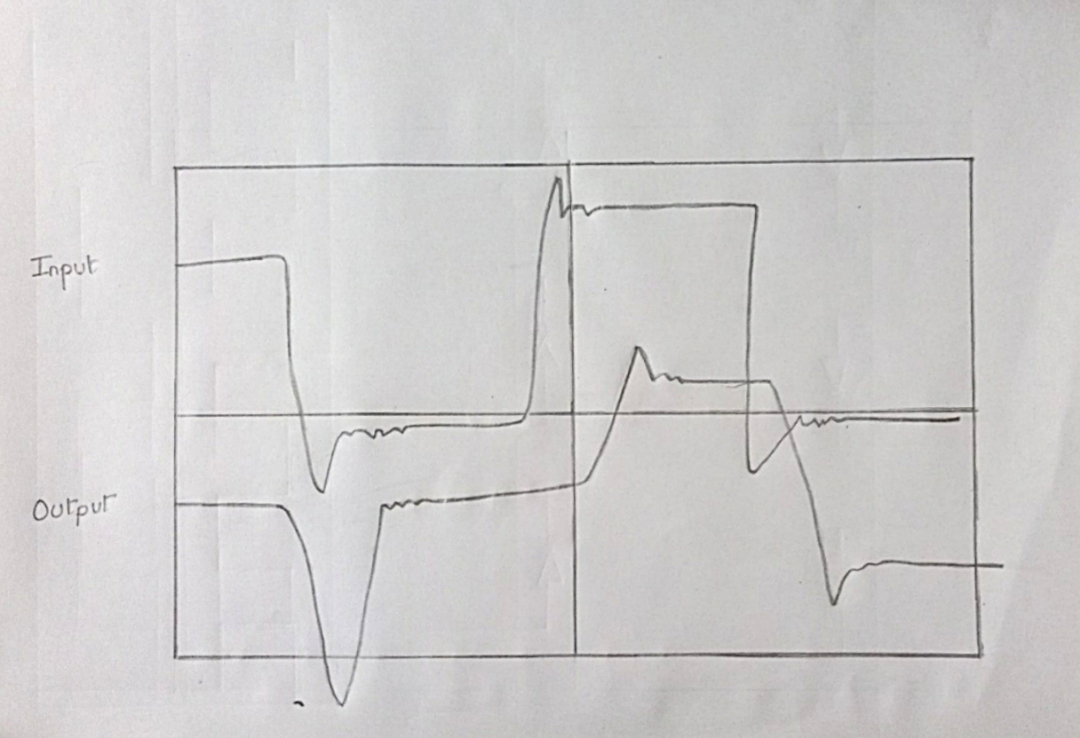
**Q:** Define Propagation delay time?

**A: It is the time taken for a signal to reach output destination from input.**

**Q:** Draw the I/P and O/P wave form.

**A:**

**Input and output:**

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**Q:** Note down the tPHL and tPLH and calculate the propagation delay of each gate?

**A: Input clock frequency:**

**tPHL: tPLH:**

**Average propagation delay (P.D.) = (tPHL + tPLH)/2 =**

**Delay per gate = P.D./6**